ABSTRACT OF THE DISCLOSURE

A programmable synchronizer system for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain, wherein the core clock domain is operable with a core clock signal and the bus clock domain is operable with a bus clock signal, the core and bus clock signals having a ratio of N core clock cycles to M bus clock cycles, where $N/M \geq 1$. A first synchronizer is provided for synchronizing data transfer from a core clock domain logic block to a bus clock domain logic block. A second synchronizer is operable to synchronize data transfer from the bus clock domain logic block to the core clock domain logic block. Control means are included for controlling the first and second synchronizers, the control means operating responsive at least in part to configuration means that is configurable based on skew tolerance and latency parameters.